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(54) **Name of Invention:** Semiconductor Device and its Method of Manufacture

(57) **Summary**

Purpose: This invention has the purpose of providing a semiconductor device that can prevent electrical leaks or short circuits between the second metal wiring (upper wiring layer) and silicon wiring or a silicon substrate installed under a through hole.

Makeup: In a semiconductor device having

- Insulating film 4 formed as an element on semiconductor substrate 1,
- 1st metal wiring layer 5 on insulating film 4,
- 2nd insulating film 6 on substrate 1 including this 1st metal wiring 5,
- 2nd metal wiring 8 on part of this 2nd insulating film 6 and
- Through hole 7 on 1st metal wiring 5 for connecting that to 2nd metal wiring 8,

A layout rule allowing this through hole 7 to extend beyond the connecting width of 1st metal wiring 5 and an opening wherein the part of through hole 7 formed by over-etching is opened up to give it a taper of 88 degrees or less.

Scope of Patent Application

Application Item 1: A semiconductor device characterized by having

- Insulating film 4 formed as an element on semiconductor substrate 1,
- 1st metal wiring layer 5 on insulating film 4,
- 2nd insulating film 6 on substrate 1 including this 1st metal wiring 5,
- 2nd metal wiring 8 on part of this 2nd insulating film 6,
- Through hole 7 on above-noted 1st metal wiring 5 for connecting that to above-noted 2nd metal wiring 8,
- A layout rule allowing above-noted through hole 7 to extend beyond the connecting width of above-noted 1st metal wiring 5,
- The upper part of above-noted through hole 7 shaped to be nearly vertical and
- The lower part of the above-noted connecting hole formed by over-etching is made so as to have a taper.

Application Item 2: The semiconductor device described in Application Item 1, which is characterized by the above-

noted connecting hole being opened so that the taper of its lower part formed by over-etching will have a taper of 88° or less.

Application Item 3: The semiconductor device as described in Application Item 1 or 2, which is characterized by the above-noted 1st metal wiring being formed so as to have a taper of 88° or less.

Application Item 4: The semiconductor device described in Application item 1 or 2, which is characterized by the above-noted connecting hole having a taper angle up to 88° in its lower part at least from the height where it touches the above-noted 1st metal wiring and having a taper angle of 88° or more upward from that position.

Application Item 5: In a method for fabricating a semiconductor device having

- An insulating film made as an element on a semiconductor substrate,
- A 1st metal wiring layer on this insulating film,
- A 2nd insulating film on the above-noted substrate, including this 1st metal wiring,
- A 2nd metal wiring on part of the above-noted 2nd insulating film,
- A through hole on the above-noted 1st metal wiring for connecting that to the above-noted 2nd metal wiring and
- A layout rule allowing the above-noted through hole to extend beyond the connecting width of the above-noted 1st metal wiring,
- The upper part of above-noted through hole shaped to be nearly vertical and
- The lower part of the above-noted connecting hole formed by over-etching being made to have a taper,

A method of manufacturing a semiconductor device that is characterized both by the plasma etching's pressure for opening up the above-noted connecting hole being changed at least two or more times so as to make the upper part of the connecting hole nearly vertical in shape, and by giving the above-noted connecting hole a taper by over-etching.

Application Item 6: In a method for manufacturing a semiconductor device having

- An insulating film formed as an element on a semiconductor substrate,

- A 1st metal wiring layer on the above-noted insulating film,
- A 2nd insulating film on the above-noted substrate, including this 1st metal wiring,
- A 2nd metal wiring 8 on part of this 2nd insulating film,
- A through hole 7 on the above-noted 1st metal wiring for connecting that to the above-noted 2nd metal wiring,
- A layout rule allowing the above-noted through hole to extend beyond the connecting width of the above-noted 1st metal wiring,
- The upper part of above-noted through hole shaped to be nearly vertical and
- The lower part of the above-noted connecting hole formed by over-etching being made to have a taper,

A method of manufacturing a semiconductor device that is characterized by opening up the above-noted connecting hole by repeated plasma etching to open the hole, changing the etching gas flow ratio two or more times to open the above-noted connecting hole and to form a taper at the bottom part of the hole by over-etching.

Application Item 7: In a method for manufacturing a semiconductor device having

- Insulating film formed as an element on a semiconductor substrate,
- A 1st metal wiring layer on the above-noted insulating film,
- A 2nd insulating film on the above-noted substrate, including this 1st metal wiring,
- A 2nd metal wiring on part of this 2nd insulating film,
- A through hole on the above-noted 1st metal wiring for connecting that to the above-noted 2nd metal wiring,
- A layout rule allowing the above-noted through hole to extend beyond the connecting width of the above-noted 1st metal wiring,
- The upper part of above-noted through hole shaped to be nearly vertical and
- The lower part of the above-noted connecting hole formed by over-etching made so as to have a taper,

A method of manufacturing a semiconductor device that is characterized by doing plasma etching with a gas system that includes hydrogen, fluorine and carbon but not oxygen so as to open the above-noted connecting hole, and doing plasma etching at a location below that with a gas of carbon, hydrogen and fluorine and a gas not including oxygen to open

the connecting hole so as to give a nearly vertical shape to the upper part of the connecting hole and form a taper on its lower part.

Application Item 8: The method for manufacturing the semiconductor device described in any of Application Items 5~7, which is characterized by the above-noted over-etched opening being formed by etching to have a taper angle of 88° or less.

Detailed Explanation of Invention

0001 Field for Commercial Utilization: This invention relates in particular to a semiconductor device and to its method of manufacture, having a layout rule that allows the connecting hole (hereafter called a through hole) connecting the metal wiring to extend beyond the width of the lower metal wiring.

0002 Usual Technology: With the higher integration and miniaturization of semiconductor devices, multi-layered structures are generally being adopted for semiconductor device wiring techniques; and a zero leeway is being sought for the layout rules for superimposing the through hole on the 1st wiring in which the hole is opened.

0003 Figure 8 is a schematic cross-sectional diagram of one example of a semiconductor device in which a multi-layered wiring structure has been adopted. As the figure shows, this type of semiconductor device has a silicon oxide field oxide film 2 on a semiconductor substrate of silicon or the like and a gate electrode 3 of polysilicon or the like. Also, the material 3' of the gate electrode is used at the same time as wiring on field oxide film 2. Also, 1st insulating film 4 of silicon oxide or the like is formed over the entire surface of substrate 1 including gate electrode 3 and gate electrode material 3'; and 1st metal wiring 5 (lower wiring) of aluminum or the like is made on top of that. 2nd insulating film 6 of silicon oxide or the like is made on substrate 1 including this 1st metal wiring 5. 2nd metal wiring 8 (upper wiring) is formed on this 2nd insulating film 6 of a material and with a makeup nearly the same as 1st wiring film 5.

0004 2nd metal wiring 8 and 1st wiring 5 are electrically connected via through hole 7.

0005 Yet, as shown in Figure 8, through hole 7 sometimes protrudes beyond the width of 1st metal wiring 5 due to such things as positioning slips while transferring mask patterns for making the through hole; and that may cause failures from short circuits or leaks via through hole 7 between 2nd metal wiring and silicon substrate 1 or polysilicon wiring 3' accidentally positioned under 1st metal wiring 5.

0006 As a means for resolving the above-noted problem, the method illustrated in Figure 9 has been proposed. As the figure shows, this method would form sidewall spacer 9 of an amorphous silicon film or the like having etching selectivity with generally used silicon oxide film, actually widening 1st metal wiring 5 so that through hole 7 does not cause short circuiting between polysilicon wiring 3' accidentally positioned under 1st metal wiring 5 or silicon substrate 1.

0007 On the other hand, when embedding 2nd metal wiring in the through hole by using high-temperature sputtering of the metal or a metal reflow, the through hole will be formed with an 85-degree taper, thus improving the wiring's coverage rate. But, in such case the taper angle within the through hole is usually formed at a set angle.

0008 The taper angle becomes smaller with a through hole dimension of 5μm or less as miniaturization of semiconductor devices advances. And, when the leeway for superimposing the through hole and the 1st metal wiring is made zero and the through hole has a set taper angle of 80°, the through hole's surface area for connecting with 1st metal wiring becomes smaller, increasing the contact resistance of the through hole and 1st metal wiring, thus risking hindering the semiconductor's high-speed operation.

0009 A method for controlling any shape for the through hole's taper was reported in Patent Release Hei.4-167524. This method uses a mixture of CHF_3 and CF_4 to etch the through hole, with the ratio of the gas flow rates being altered as the etching proceeds so as to forma hole of any taper shape. I.e., by altering the ratio of CF_4 continuously from 100% to 10% and then 50%, the hole's shape will be processed to a taper at the top and a vertical shape at the bottom.

0010 Issues the Invention Seeks to Resolve: As described above, if one forms a sidewall spacer on the side surfaces of 1st metal wiring, the space between the 1st metal wiring essentially become narrower and that reduces the step

coverage margin for the 2nd insulating film, creating such problems as hindering the miniaturizing of the semiconductor device. Also, in forming the sidewall spacer, there have been anticipated difficulties in the rising cost of adding such processes as forming the amorphous silicon sidewall spacer and doing the etch-back after making 1st metal wiring, all of these lowering the through-put.

0011 Also, with the above-described approach of controlling the hole's shape by continuously altering the gas flow ratios, when the size of the hole is miniaturized to 0.5μm or less due to the advance of semiconductor miniaturizing, the contact area with the lower metal wiring decreases, raising contact resistance and possibly obstructing the high-speed operation of the semiconductor device.

0012 Moreover, since one is making the gas flow ratio change continuously, control of the gas flow meter becomes difficult, making control of the shape difficult also.

0013 This invention was devised to resolve the above-described usual problem points and has the purpose of preventing electrical leaks or short circuits between the 2nd metal wiring and either the silicon wiring or the silicon substrate located under the through hole.

0014 This invention also has the purpose of preventing increases in contact resistance between the through hole and the 1st metal wiring so as to enable high-speed operation of the semiconductor device.

0015 Means to Resolve the Problems: In a semiconductor device having

- A 1st insulating film on a semiconductor substrate on which elements are formed,
- A 1st metal wiring on part of this 1st insulating film,
- A 2nd insulating film over the substrate including this 1st metal wiring,
- A 2nd metal wiring on part of this 2nd insulating film,
- A connecting hole in the above-noted 1st metal wiring for connecting the 1st metal wiring and 2nd metal wiring and
- Having a layout rule allowing for this connecting hole to extend beyond the connecting width of the above-noted 1st metal wiring,

This invention is characterized by the upper part of the above-noted connecting hole having an almost vertical shape and its lower part having a tapered shape formed especially by over-etching.

0016 Also, it is best to make the above-noted connecting hole have a taper angle of 88° or less.

0017 Again, it is best to form the above-noted 1st metal wiring with the same taper angle.

0018 Furthermore, it is best for the above-noted connecting hole to have a taper angle of up to 88 degrees at its lower part at least from the height where it contacts the above-noted 1st metal wiring and a taper angle of over 88 degrees upward from that position.

0019 The first method for manufacturing this invention is characterized by opening the above-noted connecting hole by repeatedly applying the etching pressure of plasma etching in two or more stages of over-etching so as to form its opening with a taper angle of 88° or less.

0020 Also, the 2nd method of manufacturing this invention is characterized by changing the etching gas flow ratios two or more times in the plasma etching for opening the above-noted connecting hole so as to form an over-etched opening with a taper angle of 88° or less.

0021 The 3rd method of manufacturing this invention is characterized by doing the plasma etching for opening the above-noted connecting hole from the point where it contacts the above-noted 1st metal wiring by using a gas containing hydrogen, fluorine and carbon but not oxygen, and at positions lower down doing the plasma etching to open the connecting hole with a gas system of one containing carbon, fluorine and hydrogen and one containing oxygen.

0022 Effects In the semiconductor device of this invention the lower part of the through hole—i.e., the part formed by over-etching has a taper so that with a taper angle of 88° or less, the surface area will be small at the bottom of the hole that is exposed to the over-etching plasma. And, with the micro-loading effect, one keeps the through hole from reaching as far as the polysilicon wiring or the substrate and thus prevents electrical leaks or short circuits of the polysilicon wiring or substrate.

0023 Also, because one forms a taper angle of less than 88° on the 1st metal wiring, the area of the hole bottom is even smaller; and the action of the micro-loading effect keeps the through hole from reaching as far as the polysilicon wiring or substrate and so prevents electrical leaks or short circuits with the polysilicon wiring or substrate.

0024 Because the through hole has a nearly vertical form at the top from the point where it contacts 1st metal wiring, its diameter will be no smaller than the designed size in the layout rules for contacting the 1st metal wiring. As noted above, that makes it possible to prevent electrical leaks and short circuits with the polysilicon wiring or the substrate, to reduce contact resistance as miniaturization of semiconductor devices proceeds and so to enable high speed operation of the semiconductor.

0025 Again, by etching with a gas containing oxygen, such as O_2, CO or CO_2, the micro-loading effect is greater for obtaining an identical taper as compared to forming the hole with gases not containing oxygen; and it makes the etching speed at the bottom of the through hole even lower, allowing even more reliable control against electrical leaks at the polysilicon wiring or substrate.

0026 Application Examples I will explain this invention while referring to the figures. Identical keying symbols are applied to the same parts as in the usual case.

0027 Figure 1 is a schematic cross-sectional diagram showing the basic makeup of the first application example of this invention. As Figure 1 shows, the semiconductor device of this invention has field oxide film 2 of SiO_2 and polysilicon gate electrode 3 arrayed on a semiconductor substrate of silicon or the like. Material 3′ of this gate electrode serves at the same time as wiring on field oxide film 2. 1st insulating film 4 is formed of silicon oxide or the like over the whole surface of substrate 1 including these elements, and then 1st metal wiring 5 is laid onto that. This 1st metal wiring 5 normally is made up of aluminum, its alloy or an alloy of multiple high-fusion metals, or even of multi-layered metal wiring.

0028 2nd insulating film 6 is formed of silicon oxide over substrate 1 including this 1st metal wiring 5. This 2nd insulating film 6 may be made in part of such insulating film as

silicon nitride. 2nd metal wiring 8 is formed on this 2nd insulating film 6 and consists of material nearly identical to that of the afore-noted 1st metal wiring 5.

0029 Then, so as to electrically connect 2nd metal wiring 8 with 1st metal wiring 5, through hole 7 is made in 1st metal wiring by plasma etching for which prescribed reactive gases are introduced. At this point, the layout rules allow for this through hole 7 to extend beyond the width of 1st metal wiring 5.

0030 Now, through hole 7 in this invention has a different taper angle at the top where in contacts 2nd metal wiring 8 from its taper angle at the bottom where it contacts 1st metal wiring 5, as it is made so that its taper angle ($\theta 2$) at the lower part 7a where it is formed by over-etching is less than 88°.

0031 Through hole 7 for this invention, as noted above, can be made so that at least part of it has a taper of under 88° due to switching the plasma in multiple stages during formation of the through hole. I will explain this method of making the through hole.

0032 Detecting the end point of through hole 7's etching by plasma etching is done by luminosity monitoring as generally practiced. At the point when the etching of 2nd insulating film 6 is nearly finished above 1st metal wiring 5, the etched matter—the source of the luminosity—decreases in volume, enabling one to detect the end of the etching. Ordinarily, when this etching end point is detected, one goes on to over-etch 30~100% in consideration of etching uniformity and differences in film thickness due to 2nd insulating film 6's pattern arrangement. Because of this over-etching, through hole 7, extending beyond the width of 1st metal wiring 5, will be more deeply etched; and, as shown in the previously discussed Figure 8, there is a risk of leaking at the polysilicon wiring or the substrate.

0033 So, with this invention one switches the etching conditions when one detects the etching end, thus reducing the taper angle of the over-etched part 7a of through hole 7's lower part and keeping through hole 7 from reaching the polysilicon wiring or the substrate. One can vary the taper angle of through hole 7 by changing the etching pressure, the ratio of etching gas flow volumes or the kinds of etching gases.

0034 Figure 2 shows an example of the makeup of the above-noted invention with the actual design dimensions adopted.

0035 This yields a semiconductor device with a 1st metal wiring 5 of 0.60μm width, a through hole 7 diameter of 0.60μm, a flattened 2nd insulating film 6 of 0.50μm on 1st metal wiring 5 and 1.00μm elsewhere and through hole 7 extending 0.3μm beyond 1st metal wiring 5 as provided in the layout. By switching the etching of through hole 7 in two stages in this semiconductor device, the upper position of 1st metal wiring 5 gets an angle of nearly 90°, while at its lower, over-etched part the hole shape has a taper of about 75°.

0036 At this point, the part of the hole extending above 1st metal wiring 5 becomes smaller at the bottom as the over-etching progresses. Due to this reduction, called the micro-loading effect, etching of the bottom surface becomes restricted and so limits the occurrence of leaks by silicon substrate 1 or polysilicon wiring 3'.

0037 Next, I will explain a second application example of this invention, while referring to Figures 3 and 4. Figure 3 is a schematic cross-sectional diagram showing the makeup of this invention's 2nd application example, while Figure 4 is a cross-sectional diagram of its main parts. This 2nd application example has the same makeup as the above-noted application example except for the shape of 1st metal wiring 5. To avoid duplicative explanations, I will skip any explanation of identical parts carrying the same keying symbols.

0038 As Figures 3 and 4 show, this 2nd application example has a taper angle less than 88° (θ3) on 1st meal wiring 5. To form a taper angle of less than 88° on 1st metal wiring 5, one limits the RF power in the plasma etching to form the wiring, which is possible by using depositing gases such as silicon tetrachloride $SiCl_4$) or ammonia (NH_3).

0039 Figure 5 shows the example actually used, with its design dimensions. The width of 1st metal wiring 5, diameter of through hole 7, thickness of 2nd insulting film 6 (on 1st metal wiring 5 and other locations), the amount by which through hole 7 extends beyond 1st metal wiring 5 and the taper angles of through hole 7 are all the same as in the 1st application example.

0040 In the patterned etching of 1st metal wiring 5, I used silicon tetrachloride, which is depositing, so as to get a tapered shape of about 80° (θ3) for this metal wiring 5. At this time, through hole 7 where it extends above 1st metal wiring (over-etched part 7a) becomes smaller toward the bottom as the etching proceeds; and, due to the micro-loading effect, it becomes constricted as etching of the bottom surface proceeds, limiting the occurrence of leaks at silicon substrate 1 or polysilicon wiring 3'.

0041 This effect makes the bottom surface even smaller than in the first application example, so that it can even better limit leaks than does the 1st application example.

0042 Next, I will use Figures 6 and 7 to explain the 3rd application example of this invention. This 3rd application example is identical to the above-noted application examples except for the shape of through hole 7. To avoid duplica-ive explanations, I will omit describing identical parts carrying the same keying symbols.

0043 As shown in Figures 6 and 7, this 3rd application example has a through hole 7 shape with a taper angle of more than 88° (θ1) in the part above the point where it contacts 1st metal wiring 5, while the over-etched part 7a below metal wiring 5 has a taper angle (θ2) of less than 88° so that through hole 7 is made with differing taper angles.

0044 Giving through hole 7 a shape in which its part above where it contacts metal wiring 5 has a taper angle (θ1) of more than 88° makes the diameter of through hole 7 where it contacts metal wiring 5 larger than when that angle is smaller. That enables reduction in the contact resistance as semiconductor device miniaturization proceeds and makes fast operation of the semiconductor device possible.

0045 The following demonstrates the effectiveness of having the above-noted taper angle (θ1) of through hole 7 at over 88°. As semiconductor devices grow even more miniaturized hereafter, through hole diameters will be miniaturized to less than 50μm. So, for instance, when 1st metal wiring 5 is 0.50μm wide, through hole 7's diameter is 0.50μm, flattened 2nd insulating film 6 is 0.50μm on 1st metal wiring 5 and 1.00μm elsewhere, through hole 7 extends 0.20μm beyond 1st

metal wiring 5, giving it a taper angle (θ1) of 80°. Then its diameter where it contacts 1st metal wiring 5 will be 20μm, whereas with a taper angle (θ1) of 80°, through hole 7 will have a diameter of about 0.29μm where it contacts 1st metal wiring 5. With miniaturization progressing to where it will have a diameter of about 0.1μm, the difference in contact surface area will greatly affect contact resistance. Then making the taper angle (θ1) more than 88° will make high-speed operation of the semiconductor device possible.

0046 Next, I will explain the method of fabricating this semiconductor device.

0047 First, the 1st method is done by monitoring luminosity in the plasma to detect the end point of generally performed plasma etching in forming through hole 7. At the point when 2nd insulating film 6 is almost fully etched above 1st metal wiring 5, the etched material—the source of the luminosity—decreases in volume, indicating the end of the etching. By controlling etching pressure so that it differs before and after detection of this end of the etching, one controls through hole 7's taper angles θ1 and θ2, as shown in Figures 6 and 7. This plasma etching mode and the pressure range will differ by the device used, but when one applies the usual pressure range of over 100mTorr, the lower one makes the etching pressure, the smaller the taper angle will become.

0048 The second method also employs monitoring of the luminosity in the plasma. Just as in the above-noted method, one detects the end point of the etching when the source of the luminosity—the etched material—decreases. By controlling the ratio of etching gas volumes before and after detecting this end point, one controls taper angles θ1 and θ2 of through hole 7, as seen in Figures 6 and 7.

0049 When etching the silicon oxide film ordinarily used as 2nd insulating film 6, one generally etches with a mixture of such a depositing gas as CHF_3 and such etching gases as HF_4 or C_2F_6; but the higher the proportion of the depositing gas is, the smaller the taper angle will become.

0050 Just as in the above-noted methods, the 3rd method does luminosity monitoring of the plasma generally used to form the through hole. When etching of 2nd insulating film 6 is nearly done above 1st metal wiring 5, the monitoring detects

a quantitative decrease in the etching material that is the source of the luminosity. For etching before detection of this end point, one does etching with a gas such as CHF_3 that includes hydrogen, fluorine and carbon plus a gas without oxygen, such as CF_4 or argon. And for the etching after detecting the etching end point, one etches with a gas containing hydrogen, fluorine and carbon, such as CHF_3 plus a gas containing oxygen such as O_2, CO or CO_2.

0051 For the etching after reaching the end point, one may also add such a gas without oxygen as CF_4. By controlling the etching gases as noted above, one controls the taper angles θ1 and θ2 of the through hole as shown in Figures 6 and 7. When etching with gases containing oxygen, such as O_2, CO or CO_2, the micro-loading effect is large for getting identical taper angles, as contrasted to when etching with gases not containing oxygen. That slows the etching speed at the through hole's bottom surface and so is effective in suppressing the occurrence of leaks at the polysilicon wiring or the silicon substrate.

0052 **Invention'sEffectiveness** As explained above, with the semiconductor device of this invention the through hole has a nearly vertical shape above where it contacts the 1st metal wiring, while its lower part—i.e., the part formed by over-etching—the taper shape formed by over-etching has a taper angle of 88° or less. So, the area of the hole's bottom area exposed to the over-etching plasma is small and the effect of micro-loading prevents the through hole from reaching the polysilicon wiring or substrate and so prevents electrical leaks or short circuits at the polysilicon wiring or substrate.

0053 Also, because the diameter of the through hole where it contacts the 1st metal wiring does not drop below the designed dimension of the layout rules, contact resistance decreases as miniaturization of the semiconductor device advances, making high speed operation of the semiconductor device possible.

0054 Moreover, since the 1st metal wiring is formed with a taper angle of under 88°, the surface area of the hole bottom becomes small and the micro-loading effect keeps the through hole from reaching as far as the polysilicon wiring or the substrate, preventing electrical leaks or short circuits at the polysilicon wiring or substrate.

0055 By forming a taper angle of over 88° above where 1st metal wiring is contacted, one gives the through hole a large diameter at that height compared to when the taper angle is smaller; and that reduces contact resistance as miniaturization of the semiconductor device proceeds, enabling it to operate at high speed.

0056 Forming the through hole by etching with such gases containing oxygen as O_2, CO and CO_2 gives a large micro-loading effect when getting identical taper angles, as compared to when forming the hole with gas not containing oxygen, thus further reducing the etching speed at the bottom of the through hole. So, one can reliably prevent the through hole from reaching the polysilicon wiring or substrate and prevent the occurrence of electrical leaks at the polysilicon wiring or substrate.

Simple Explanation of Figures

Figure 1 is a schematic cross-sectional diagram showing the makeup of the 1st example of applying this invention.

Figure 2 is a schematic cross-sectional diagram showing an example of adopting the actual designed dimensions in the 1st application example.

Figure 3 is a schematic cross-sectional diagram showing the makeup of the 2nd application example of this invention.

Figure 4 is a cross-sectional diagram of the main parts of this invention's 2nd application example.

Figure 5 is a schematic cross-sectional diagram showing an example of adopting the actual designed dimensions in the 1st [*sic*] application example of this invention.

Figure 6 is a schematic cross-sectional diagram showing the makeup of a 3rd application example of this invention.

Figure 7 is a cross-sectional diagram of the main parts of this invention's 3rd application example.

Figure 8 is a schematic cross-sectional diagram showing one example of a semiconductor device using a multi-layered wiring structure.

Figure 9 is a schematic cross-sectional diagram showing one example of a semiconductor device using a sidewall spacer.

Explanation of Keying Symbols

1	Substrate
2	Field oxide film
3	Gate electrode
3′	Gate electrode material wiring)
4	1st insulating film
5	1st metal wiring (lower wiring)
6	2nd insulating film
7	Through hole
8	2nd metal wiring (upper wiring)